REMARKS

These remarks are in response to the third non-final substantive Office Action of December 15, 2006. The Office Action rejected claims 1-7, 9-20, 22-39, 52-58, 61-65, 76, 77, and 91-110 under 35 USC 103(a) as being unpatentable over Chen et al., "A Unified Compact Scalable Model for Hot Carrier Reliability Simulation" in view of Kadoch et al. (US patent 5,761,481) and further in view of Rajgopal et al. (US patent 6,363,515). It is respectfully submitted that these rejections are in error.

Concerning the Kadoch reference, it is respectfully submitted that Office is misapplying this reference and makes several mistakes in interpreting it. Consequently, it seems sensible to start with a rather detailed discussion of the Kadoch reference. The heart of the Kadoch process is described there with respect to Figures 5-7 at column 6, line 11, to column 8, line 14. Figure 5 is a flow chart on Kadoch's method, Figure 6 is an experimental tree that illustrates some of the details in the flow of Figure 6, and Figure 7 provides detail on step 512 of Figure 5.

The flow Kadoch presents in Figure 5 begins with defining the various inputs that will be used in simulating *half* of a MOS transistor. The steps 502-508 all relate to assembling the information that will be used in step 510 when a process simulation is run; however, it needs to be noted that this first run of simulation is not even for the MOS device as a whole, but just for the *half structure* that Kadoch introduces. This is described, for example, at column 6, lines 16-18: "In step 502 the process input deck 22 is defined so that *when it is executed* by the process simulator 30 a *half structure* of a MOS transistor *is generated*." As the added emphasis shows, Kadoch's process is all based on first executing a simulation for this half-structure. This can also be seen by looking at Figure 5 itself, where each of steps 502-508 relate to the half structure and 503 and 505 are corresponding schematic illustrations.

Although Kadoch is concerned with simulating the operation of MOS devices for various channel length, the basis of this method is the use of the half structure. This idea is that much of the important behavior of a MOS is due to what goes on at or near the source/drain regions. The half structure covers these regions and a simulation run for the half structure will account for a major portion of the MOS properties. These results are then adjusted, based on a subsequent simulation run, for a specific channel length.

Kadoch's Figure 6 shows a process tree related to step 508. As shown there, the initial half structure simulation is performed and then, at 608, a specific channel length needs to be specified. This is in contrast to Figure 16, which is a prior art method that requires the channel length be specified at the outset prior to the simulation. In contrast, Kadoch allows much of the aspects of the simulation related to the source/drain regions, and which are not so dependent on channel length, to be done once, using the half-structure he introduces for this purpose. In any case, however, Kadoch *requires a simulation run just for this half-structure alone*, before a desired channel length is specified.

Step 510 ("run process simulator to simulate fabrications of the half structure ...") is when the simulation is run for the half structure. This is described at column 7, lines 2-6: "In step 510, the tool 12 *runs the process simulator* 30 *to simulate the transistor half-structure* utilizing the defined process input deck 22 and the defined process parameter matrix 20." Thus, as the added emphasis indicates, Kadoch already requires a first simulation run *before a specific channel length is input.*

In step 512, a channel length is then needed to be prescribed. Figure 7 provides detail on step 512. As noted at column 7, lines 18-20: "In step 704 a *prescribed, or 'target' channel length (L) is input* from the channel length data 24 to the channel length selector 34", where the emphasis is added. Kadoch's process then determines, based upon this prescribed length, how to expand the half structure simulation to the full structure. As described in Figure 7 and its description (column 7, beginning at line 13), this all very specific to the fact that this is being done for a single device and that this is a MOS transistor. This allows a half-structure simulation run done for one source/drain region to be mirrored for the other source drain region, followed by any needs revisions for actual specified channel length.

Once the structure is then expanded for the prescribed channel length, *another simulation is then performed at step 514*: "run device simulator to simulate electrical properties ... of the full structure ...". As then noted at column 7, lines 60-62: "The result of the foregoing is the generation of a full structure of the prescribed target channel length." Consequently, before going on to output the results to the user at steps 516 and 518, Kadoch requires an additional simulation run for each specified length.

Thus, not only does Kadoch ***not*** determine the operation of a MOS for multiple channel lengths in single run, but Kadoch require *multiple* runs even for a *single* specified channel length: a first run (step 510) is needed for the half structure and additional runs (step 514) are needed for each prescribed channel length. This single, half-structure run can then be used for the different specified channel lengths, but it is only for the half-structure: it subsequently needs to be expanded to the full structure of the prescribed lengths. This is also believed clear form a close reading of Kadoch's Summary: see, for example, column 2, lines 34-35 ("followed by separate computations to expand the half structure to a full structure"), lines 50-55 ("A process simulator simulates fabrications of a half-structure ... . A channel length selector then expands the half-structure fabrications to full structure fabrications of prescribed channel length. A device simulator then simulates ..."), and so on.

Kadoch teachings are also very specific and limited to a *single* MOS device and to variations due to *channel length*. (In its title and descriptions, Kadoch is even specific as to this being for N-channel devices.) A MOS transistor structure consists of a pair source/drain regions separated by a channel region. Kadoch relies upon this structure to split the device in half and then look at a single source drain region with a portion of the channel attached. Since a significant portion of the properties of a MOS, particularly those properties with which Kadoch is concerned, relate to what goes on at and adjacent to the source/drain region, Kadoch then runs a simulation just for this half structure. Then, based precisely on this being a MOS device and that he is looking at variations in channel length, Kadoch is then able to mirror the result for the one source/drain regions to obtain the properties for both source/drain regions, tie these two together to obtain a whole device, then compensate for the actual, prescribed channel length. These teaching are all highly specific and limited to a single MOS device and to variations in channel length and are not extendable to a whole circuit and to the process of circuit degradation with time as the sort of symmetries and relationships upon Kadoch relies are lacking.

This has been a rather long, and somewhat repetitive, digression on the Kadoch reference; however, based on the "Response to Arguments" portion of the Office Action with respect to claim 1 (page 14), it appears that the Office Action is taking the Remarks of the previous Response as type of argument that is just quibbling over how obvious is obvious. As can been seen from the preceding discussion, it is instead believed that what the Kadoch patent is

doing is quite different than what would be applicable here and is being improperly applied in the rejection of the current claims. Kadoch exploits the physical properties and symmetry of a single MOS device to split the transistor down the middle and simulate this half-structure, which can then be mirrored for the whole structure; it is unclear how would this could be applied to the degradation process of a circuit where the state of the circuit lacks any obvious analogue of the physical symmetry properties of a MOS and where the degradation process is something that proceeds in a monotonic manner with time. Consequently, it is respectfully submitted that not only is it ***not*** obvious to apply such teachings to claim 1, but, even were one to try to apply such teachings to the present invention, it unclear how one would proceed to do so. Further, Kadoch *does* ***not*** *disclose simulating, in a single run, the operation of the MOS for multiple channel lengths*; rather, as discussed above, even for a single MOS and for channel length, Kadoch requires a first run just for the half-structure follow by an additional run for each specified channel length. Thus, not only is it not obvious how to extend the teachings of Kadoch to the present invention, but the Office Action has yet to make the necessary *prima facie* case for the rejection of the pending claims.

Claims 1-7

Turning to the claims, claim 1 is drawn to an aspect of the present invention that allows for simulating for multiple stress time values in a single run, as is described, for example, beginning on line 7 of page 8 of the present application. It is respectfully submitted that such a method is neither taught nor suggested by Chen, Rajgopal, or Kadoch, either alone or in combination. In its rejection of claim 1, the Office Action relies upon Chen for the majority of claim elements, with Rajgopal cited for the netlist. Kadoch is cited only at column 2, line 62, and only for the "simulating in a single run" limitation. The Office Action is correct in that neither Rajgopal nor Chen allow for simulating for multiple stress time values in a single run; but, as discussed in the preceding, neither does Kadoch.

As discussed above, it is respectfully submitted that the Office Action is misreading and misapplying the Kadoch reference: Kadoch does not teach the simulation for multiple channel lengths in a single run; rather, even for a single prescribed channel length, Kadoch requires multiple simulation runs, a first run for just the "half-structure" introduced there and a second

run for each prescribed length. Further, the teachings of Kadoch are so specific and tied the case of a single MOS device and channel length that even if Kadoch were to teach "simulating in a single run" (as incorrectly asserted by Office Action), it is respectfully submitted to be unclear and highly non-obvious how this would be applied to the limitations of claim 1.

More specifically, claim 1 has as its second element:

> supplying a plurality of circuit stress time values;

and ends with

> determining degraded operation of the circuit by *simulating in a single run operation of the circuit* with the specified components using their respective aging model information and respective relative component degradation parameter *at the plurality of supplied circuit stress time values.*

The emphasis has been added. For the "simulating in a single run operation of the circuit", the Office Action cites Kadoch at column 2, line 62, which refers to "a single run of a process simulator to produce simulations of structures of varying channel lengths". However, as discussed above, Kadoch's teachings are all directed to simulation of a *single device*, not a circuit of multiple components; are quite specific and tied to variations is channel length, so that it is unclear how, or even if, these would relate to the degradation level at differing time values; and it is only the early stages of Kadoch's simulation process that is for multiple channel length, as a prescribed channel length must be input at an intermediate stage and another run executed before the simulation for the device as a whole can be completed.

Finally, it should be noted that the Office Action states (end of second paragraph, page 14) that "The Office refutes this argument since it's not impermissible hindsight if the motivation to combine stems from the prior art." It is respectfully submitted that the references lack such motivation and that, in any case, the Office Action does not provide it. As discussed at length, the teachings of Kadoch are all highly specific and dependent upon their application to a single MOS device and channel length.

Therefore, for at least these reasons, it is respectfully submitted that a rejection of claim 1, along with its dependent claims (2-7, 9-20, 22-39, 52-58, 61-65, 76, 77, and 93-98), under 35 USC 103(a) as being unpatentable over Chen in view of Rajgopal and further in view of Kadoch is in error and should be withdrawn.

A number of these dependent claims are believed further allowable for their additional limitations. In particular, with respect to each of claims 4-7, these claims recite features that the

cited references admittedly do not disclose. Yet there is no further reference or other evidence of prior art presented to demonstrate that the overall claimed combinations including the elements missing from the cited art would have been obvious. The Office Action (page 14, line 15, to page 15, line 6) either summarily states that "it's obvious" to add the missing element, or that "one of ordinary skill ... naturally would want to" perform a particular limitation, or that "it would be obvious .... to manipulate [a] formula" in order to meet the terms of the claims. In any of these cases, assumptions have improperly been made by the Examiner as to what one ordinarily skilled in the art would have found obvious to do since there is no supporting evidence provided in the Office Action. It is respectfully submitted that these rejections do not make the necessary *prima facie* case of obviousness, and that, on that basis, the rejection of claims 4-7 must be withdrawn.

For example, claim 4 includes the further limitation of "wherein the simulating is performed using a timing simulation type circuit simulator", for which the Office Action cites Chen at page 246, figure 5, "stress time"; however, this only refers to how long the circuit has been stressed and has no reference to a timing simulation type of simulator (such as Starsim or Timemill, as opposed to a SPICE type simulator, examples being as HSPICE or Spectre). Chen does refer to SPICE modeling technology, but does not appear to disclose a timing simulation type of circuit simulator. Consequently, claim 4 is believed further allowable on this basis. (Based on the Office Actions remarks with respect to this claim in the Response to Arguments section on page 14, the Office Action seem to be confusing "timing simulation type circuit simulator" with "stress time analysis". This is incorrect: this claim refers to a class of simulators, such as Starsim or Timemill, as opposed to a SPICE type simulator, examples being as HSPICE or Spectre.)

As for claim 5, this includes the further limitation of "wherein the aging model information on the selected ones of the components is derived from electrical test data." The Office Action cites Chen for the "aging model" and Rajgopal for "selected ... components", but supplies no citation for "derived from electrical test data", which is the substance of the limitation. Consequently, the rejection is improper and claim 4 is believed further allowable on this basis.

Similarly, claim 7 includes the further limitation of "wherein determining the degraded operation of the circuit comprises determining the circuit's speed at the supplied circuit age parameters", for which the Office Action cites Chen at page 244, equation 2 with right column, lines 4-8. The cited location does refer to age, but there is no disclosure of circuit speed and, in particular, of "determining the circuit's speed".

Concerning claim 6, this contains the limitation that "said simulating the behavior of the fresh circuit" from claim 1 "determines the waveforms at the nodes to which the selected ones of the components are connected relative to an input waveform." For this additional element, the Office Action refers to Chen's figure 10, the "Fresh" curve; however, Chen's figure 10 does not show waveforms at a node relative to an input waveform or anything else, but just presents I-V curves for a fresh device and then a stressed device for a number of different gate voltages.

Claims 93 and 9-20

Claim 93 depends upon claim 1 and is believed allowable on this basis alone. Claim 93 is further drawn to an aspect of the present invention allowing different performance criteria to be applied to different circuit blocks. This is described in the paragraph beginning on page 8 at line 20. In particular, claim 93 includes:

> supplying an independent performance criterion for each set of said plurality of distinct sets of components;

The present Office Action provides no citation for this element. (The previous Office Action cites Rajgopal at column 8, lines 40-42, as does the rejection of claim 9. This cited portion of Rajgopal is a claim: "The method of claim 7 including the power use of the system that includes components and the power use of said components." This neither teaches nor suggests "supplying an *independent performance criterion* for *each set* of said plurality of distinct sets of components".

Further, the next element of claim 93 is:

> wherein said supplying aging model information includes supplying aging model information on selected components from each of said sets of components,

for which the Office Action provides no citation in any of the references and which is not believed to be found in the cited references. (In its rejection of claim 93, the previous Office Action did not include this element when it listed the claim.)

In its "Response to Arguments" section with respect to this claim (page 15), the Office Action states "Firstly, Rajgopal at least suggests this limitation", yet provides no citation to back up this assertion. The Office Action then goes on to state "Secondly, 'distinct sets of components' can be for example, 1k resistor as opposed to 100k resistor ...", which seems to reflect a basic misunderstanding of the claims: 1k as opposed to 100k are ***just different values of the same component, which is quite a different thing from "distinct sets of components"***. See, for example, the discussion in the paragraph beginning on page 8 at line 20 of the present application. The Office Action is again making improper rejections by stating that certain claim elements are "obvious" or "well known", but failing to provide a reference for this purpose. Consequently, the Office Action is again failing to even make the necessary *prima facie* case.

Consequently, for any of these reasons, a rejection of claim 93, along with its dependent claims 9-20, under USC 103(a) as being unpatentable over Chen in view of Rajgopal and further in view of Kadoch is believed to be further in error and improper on this basis.

A number of claims 9-20 are believed further allowable for their additional limitations. Concerning claims 9-20, for "distinct sets of components", the Office Action again refers to Rajgopal at column 8, lines 40-42, which was quoted above. This passage has no disclosure of "distinct sets of components", only "the system" and "components" it contains. This passage is also cited for "an analog block" and "a digital block", which are also not found there. As to the specifics of the various claims, in claim 12, for example, the Office Action provides a list of components without providing a citation for them. Concerning claim 15, the cited location of Chen does describe "forward/reverse operation", but not "driving capability" or a "performance criterion" therefor, which is what is recited in the claim. Concerning claim 16, the Office Action states "JFETs well-known", which may be true; but the claim recites "bipolar junction transistor", which a JFET is not, being instead a field effect transistor. Concerning claim 18, the Office Action provides no citation for "different models for simulating the same device type."

(In its last paragraph on page 15, with respect to some of claims 9-20, the Office Action again makes several states that again reflect a basic misunderstanding of the limitations in question and whose relevance to the actual claims in question is unclear. For example, a statement such as "Furthermore, 'different models for simulating the same type' is an intermediate step that's conducted by the user; for example, one might simulate a pair of two

stage common emitters, each having a different variable resistor." In addition to this being incorrect and improper, it again shows a misunderstanding of the claim limitations: a different resistance value for an element and using a different model for this element are two quite distinct things.)

Claims 94 and 22-39

Claim 94 depends upon claim 1 and is believed allowable on this basis alone. It is believed further allowable as it also drawn to the aspect of the present invention presented whereby the depredation level of selected components can be specified, as opposed to determining the level of degradation for other elements. This is described, for example, beginning on page 9, line 20, of the present application as part of optional step 103 in Figure 5. In particular, claim 94 includes the additional element of:

> specifying the degradation level of a second set of selected components of the circuit, wherein the elements of the first set and the second set of components are distinct,

where the degraded operation of the circuit then uses these specified values for the selected set of components, while the other set of components again uses the determined level of degradation. The current Office Action ***provides no citation for this limitation***. It is again respectfully submitted that this further limitation is neither taught nor suggest in the cited references. In its "Response to Arguments" with respect to this claim, the Office Action states (page 16): "Applicants argue that the prior art fails to disclose a 'first set' and a 'second set' of components .... In response, these devices type can be anything (i.e., transistors ...), to which each reference mentions, or at least suggests, any of these examples." This is again improper, as the Office Action is just stating that it would be obvious to do something not disclosed in the references. More importantly, this claim does not specify just splitting components up into a "first set" and a "second set" for no particular reason, but "*specifying the degradation level of a second set of selected components of the circuit*" [emphasis added] which is something that the Office Action completely ignores and for which it ***provides no citation***. This, it is again respectfully submitted that not only is this rejection incorrect, but that it is again improper. Consequently, a rejection of claim 94, along with its dependent claims 22-39, under 35 USC 103(a) as being unpatentable over Chen in view of Rajgopal and further in view of Kadoch is believed to be further in error on this basis.

Dependent claims 22-36 are drawn to various examples of what the "first set" and "second set" of components may be, and to various examples of how the degradation level may be specified. As with claims 9-20, the Office Action again cites Rajgopal, column 8, lines 40-42, for the division of components into a first and second set. As already discussed, it is again respectfully submitted that is in error. A number of claims 22-36 also believed further allowable for the additional limitations they contain. For example, claims 23 and 25 recite that the "second set of components form", respectively, "a digital block" and "an analog block", for both of which the Office Action again cites Rajgopal, column 8, lines 40-42, when neither of these are found there. For claims 31, 32, 34, and 35, see the remarks above concerning claims 15, 16, 18, and 19, respectively.

Concerning claims 37 and 39, these give specific examples of ways of specifying the level of degradation. In claim 37, "the degradation level of the second set of selected components is specified as a relative component degradation parameter with respect to the component degradation parameter of the first set of components", for which the Office Action cites Chen at page 243, left column, line 6. It is respectively submitted that the use of such a relative scale of degradation is not found in Chen at this location or, as far as can be determined, elsewhere in the cited references. In claim 39, "the degradation level of the second set of selected components is expressed in terms of lifetime", for which the Office Action cites "Chen: pg. 244, line 7", presumably the right column; however, this just states that H and m are lifetime parameters. Consequently, claims 37 and 39 are believed further allowable on this basis.

Claims 95, 96 and 52-58

Claim 95 depends upon claim 1 and is again believed allowable on this basis alone. Claim 95 is further drawn to an aspect of the present invention where multiple current sources are added to represent different degradation mechanisms, as shown in Figure 6 of the present application and described beginning on page 13, line 4, with more detail given starting in the paragraph beginning on line 17 of that page. In particular, claim 95 includes:

> revising the netlist, wherein ***each*** *of said selected components is replaced by a non-aged version of the selected component and a* ***plurality of independent current sources*** *corresponding to different mechanisms connected between the terminals of the non-aged version*, wherein a magnitude of a current relative to a circuit stress time in each of the current sources of a component is determined from the aging model

information of the component and a ***distinct*** *mechanism degradation parameter* derived from the component degradation parameter; and

wherein said determining the degraded operation of the circuit includes determining the degraded operation of the circuit by simulating the operation of the circuit with the revised netlist at the supplied circuit stress time values.

The emphases have been added to highlight those elements that particularly distinguish this claim. For "revising the netlist"; "a plurality of independent current sources corresponding to different mechanisms connected between the terminals of the non-aged version"; and "a distinct mechanism degradation parameter" the current Office Action again ***provides no citation for these limitations*** and just includes the rejection of this claim along with the rejection of claim 1.

In its "Response to Arguments" with respect to this claim (page 17), the Office Action again makes a number of remarks that are incorrect, improper, or both. The Office Action states: "The limitations of 'revising a netlist' and 'plurality of independent current sources' are common integral steps of a circuit simulation software platform i.e. SPICE to which Chen makes reference to. Each time a circuit is amended a revised net list is completed. Furthermore, it's common for circuits in today's level of intricacy to have a plurality of independent current sources." The Office Action again improperly just stating that certain elements are "common", without any substantiating reference. Further, the claim does not just state "revise a netlist" and "have a plurality of independent current sources". Both these, and the other elements of the claim, describe a specific structure and are related in a particular way:

revising the netlist, wherein each of said selected components is replaced by a non-aged version of the selected component and a plurality of independent current sources corresponding to different mechanisms connected between the terminals of the non-aged version, wherein a magnitude of a current relative to a circuit stress time in each of the current sources of a component is determined from the aging model information of the component and a distinct mechanism degradation parameter derived from the component degradation parameter; and

wherein said determining the degraded operation of the circuit includes determining the degraded operation of the circuit by simulating the operation of the circuit with the revised netlist at the supplied circuit stress time values.

Not only does the Office Action provide no references to the cited art for these elements, merely stating that they are "common", but it further ignores the specific relationships between these elements that are recited in the claim.

At line 12 on page 17, the Office Action goes on to state: "Furthermore, the Office finds little distinction between 'degraded device characteristics' and 'a distinct mechanism degradation parameter' since parameters define a characteristic of something or an event." Aside from the

relevance of the remark being somewhat unclear, it is also incorrect. Concerning different degradation mechanisms, reference is again made to Figure 6 of the present application and the description beginning on page 13, line 4, with more detail given starting in the paragraph beginning on line 17 of that page.

Consequently, for at least these reasons, a rejection of claim 95, along with its dependent claims 96 and 52-58, under 35 USC 103(a) as being unpatentable over Chen in view of Rajgopal and further in view of Kadoch is believed to be further in error on this basis.

Concerning claim 96, this further incorporates an aspect of the present invention allowing for device models to be updated. This aspect is discussed below with respect to claim 97 and the Examiner is referred to the first paragraph under the next heading. Claim 96 is further believed allowable on this basis.

Concerning claim 55, this claim further includes "determining a magnitude of a respective current in each of the independent current sources", where said determining includes "supplying a physical model of the current magnitude" and "establishing values of coefficients in the physical model from electrical test data". For "establishing values of coefficients", the Office Action refers to Chen's equation 7; however the coefficients given there are just described as fitting parameters and no disclosure is given of them being established from electrical test data. Additionally, the model presented in this section of Chen is not for the magnitude of a current source, but for current degradation, where Chen's figure 5 looks at the model for various stress times.

Concerning claims 56, this includes the limitation that the degradation level of selected components is expressed in terms of lifetime. As discussed above with respect to claim 39, the cited location of Chen just states that H and m are lifetime parameters.

Claim 58 includes that the revising of the netlist is embedded in the circuit simulator. The Office Action provides no citation for this limitation, just including it in its rejection of claim 1. (The previous Office Action referred to Rajgopal at column 5, line 63; however, this only discloses a mapped netlist, which has no such embedding of netlist revisions.) Thus, claim 58 is believed further allowable on this basis.

Claims 97 and 61-65

Claim 97 depends upon claim 1 and is again believed allowable on this basis alone. Claim 97 is further drawn to an aspect of the present invention allowing for device models to be updated, as described, for example, beginning on page 15, line 18, of the present application, and is believed further allowable on this basis. In particular, the simulating of claim 97 "includes incorporating aging of the selected components by updating the models of said circuit simulator". The current Office Action ***provides no citation for this limitation***, just including the rejection of this claim with its rejection of claim 1. (The Office Action lists claim 97 as being rejected, along with several other claims, a second time on page 11, but the additional limitations of claim 97 are also not addressed.) Consequently, the references, either alone or taken in conjunction, do not appear to disclose the updating of a circuit simulator's models as described. (In its "Response to Arguments" section with respect to claims 97 and 61-65, the Office Action states (last paragraph, page 17) that "Updating the models is an intermediate step conducted by the user"; however, the Office Action provides no citation to this effect–and in any case, the claim states that this is done as part of the simulation, not just as some intermediate step done by the user should they get the urge.) Consequently, a rejection of claim 97, along with its dependent claims 61-65, under 35 USC 103(a) as being unpatentable over Chen in view of Rajgopal and further in view of Kadoch is believed to be further in error on this basis.

Concerning claims 62 and 63, these respectively include the limitation that "incorporating the aging of the selected components comprises including the time dependence of a substrate current", and "a gate current", respectively. With respect to the "substrate current", the Office Action provides no citation for this element, only the previously used citation for "selected components". (In its "Response to Arguments" section for claims 98, 76, 77, the Office Action states "Substrate data is part of a MSOFET [sic] device, which is disclosed in Chen": Chen does disclose a MOSFET, but no citation for substrate is given and, in any case, the claim states "including the *time dependence* of a substrate current"[emphasis added], which is not disclosed.) With respect to the "gate current", the Office Action cites Chen on page 244, right column "Gate bias dependency"; however, this section concerns the gate bias dependency of the source to drain current and does not relate to "a gate current" or its time dependence. (In its "Response to Arguments" section, in the first line of page 18 the Office Action states "The Chen reference

does suggest gate current with its particular properties", but declines to provide any additional reference to this effect.) Thus, claims 62 and 63 are believed further allowable on this basis.

As for claim 64, this further includes the sub-aspect of "gradual aging", described in the paragraphs beginning on page 15, line 7, of the present application. Claim 64 includes determining an "intermediate component degradation parameter" on selected components by simulating the fresh behavior of the circuit, for which the Office Action cites Chen at page 243, left column, second paragraph, line 6. It is respectfully submitted that this cited location only contains some general comments on degradation and that there is no discussion of determining "intermediate component degradation parameters". Thus, claim 64 is believed further allowable on this basis.

(In its "Response to Arguments" section with respect to claims 97 and 61-65, beginning on line 3 of page 18, the Office Action quotes a passage of the application and then states "The highlighted areas [referring to emphasis added to the quote in the Office Action] of this passage states that the use has the ability to access the intermediate results, for selected components (Rajgopal) thus is an intermediate step to any circuit analysis program." It is unclear as to which claim or claim these comments relate and their relevance, although they seem most likely to refer to claim 64 as they follow comments related to claim 63. Besides not addressing what claim 64 is about, these comments are incorrect. The quoted portion of the application ends with the sentence "User defined ***functions*** can access intermediate results of circuit simulation": as the added emphasis indicates, this sentence states that "user defined ***functions***", not the user (as incorrectly stated in the Office Action), "can access intermediate results of circuit simulation".)

Claim 65 includes that the updating of models is embedded in the circuit simulator, similar to the aspect discussed above with respect to claim 58 for revising the netlist. The Office Action again provides no citation for "updating the models of said circuit simulator is embedded in the circuit simulator". Thus, claim 65 is believed further allowable on this basis.

Claims 98, 76, and 77

Claim 98 depends upon claim 1 and is again believed allowable on this basis alone. It is believed further allowable as it also is drawn to the "quantizing" aspect of the present invention

presented, for example, beginning on page 14, line 9, of the present application. In particular, claim 98 includes:

quantizing each of said relative degradation levels to one of a plurality of discrete values;

and then using the quantized relative degradation levels at the supplied circuit stress time values. The current Office Action ***provides no citation for this limitation***, just including the rejection of this claim with its rejection of claim 1. (The Office Action does refer to "distinct quantized (age times ...)" in its rejection of claims 64, 65, 76, 77, 91, and 97, citing Chen at page 246, figure 5. This figure does show different time values, ***but this is not the same thing as quantizing of relative degradation to a number of discreet values***.) (Concerning the "Response to Arguments" with respect to this claim that the Office Action makes on page 19, these seem to have either been misplaced from another claim or incorrectly copied here as they do not relate to limitations of claim 98.) Consequently, a rejection of claim 98, along with its dependent claims 76 and 77, under 35 USC 103(a) as being unpatentable over Chen in view of Rajgopal and further in view of Kadoch is believed to be further in error on this basis.

Claim 76 further introduces revising the netlist, as discussed above with respect to claim 95, and thus believed further allowable on this basis.

Claim 77 includes that the quantization is embedded in the circuit simulator, similar to the aspect discussed above with respect to claim 58 for revising the netlist, and thus believed further allowable on this basis.

Claims 91, 92, and 99-110

Claim 91 incorporates the limitations of claim 1. Claims 105-110 depend upon the claim 91 and further incorporate the limitations of claim 93-98. Consequently, each of claims 91 and 105-110 is believed allowable for the reasons given above for claims 1 and 93-98, respectively.

Similarly, claim 92 incorporates the limitations of claim 1. Claims 99-104 depend upon the claim 92 and further incorporate the limitations of claim 93-98. Consequently, each of claims 92 and 99-104 is believed allowable for the reasons given above for claims 1 and 93-98, respectively.

Conclusion

For the reasons given above, it is believed that the pending claims are allowable. Reconsideration of claims 1-7, 9-20, 22-39, 52-58, 61-65, 76, 77, and 91-110, is respectfully requested and an early indication of their allowability is earnestly solicited.

Respectfully submitted,

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